IP5389Register documentation

1 I2C interface

IP5389 supports LED2 LED3 multiplexing as I2C connection mode, and connect according to the corresponding method to enter I2C mode. IP5389 i2c communication frequency supports up to 250K, 8-bit register address, 8-bit register data, both sending and receiving are high-order bit first (MSB). There are 6 groups of I2C device addresses, as shown in Table 1 below.

IP5389 sets the I2C device address by judging the resistance value of the VSET (pin 41) pin connected to GND. The default address is 0XEA.

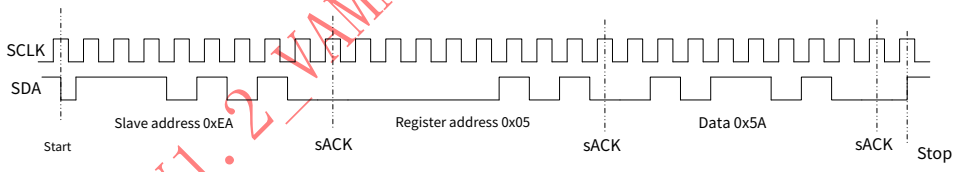
I2C device address:

Pin 41 is connected to the GND resistor. Value (ohms 1%)	I2C device address	Read as device address +1
27K	0XEA	0XEB
18k	0XE8	0XE9
13k	0XE6	0XE7
9.1k	0XE4	0XE5
6.2k	0XE2	0XE3
3.6k	0XE0	0XE1

Table 1

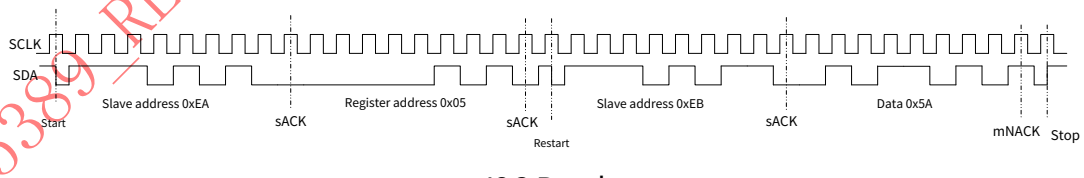
For example:

Write data 0x5A to the 0x05 register of I2C device address 0XEA,



I2C Write

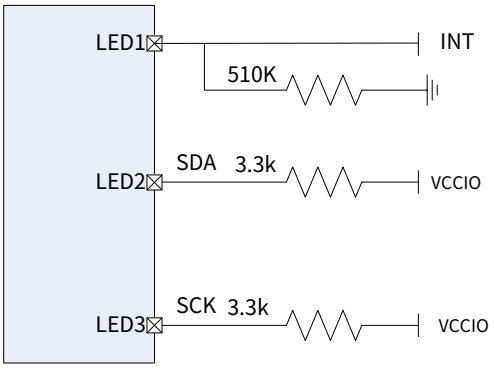
Read back data from register 0x05 at I2C device address 0XEA



I2C Read

When reading and writing registers, read and write single bytes and do not read and write continuously.

2 I2C Application Notes



IIC mode

1) INT application instructions:

When IP5389 is in sleep state, INT is high impedance. The MCU must stop accessing I2C within 16ms after detecting that INT is low. When IP5389 is in sleep state, if it detects that INT is high, it will wake up IP5389. After IP5389 wakes up, INT is Take the initiative to pull it high, and after 100ms, the MCU can start accessing I2C data; before IP5389 enters sleep, it will switch INT to input high impedance. If INT is pulled high by the MCU, it is considered that the MCU does not allow IP5389 to enter sleep.

2)**IP5389_I2C_AACC**This document register is supported, other models do not support this document register:.

3) The maximum frequency of IP5389 I2C supports 250K. Considering the MCU clock deviation, it is recommended that the clock of MCU communication be about 200K when applying I2C;

4) If you want to modify a certain register of the IP5389, you need to first read the value of the corresponding register, perform an AND or operation on the BIT bit that needs to be modified, and then write the calculated value into this register to ensure that only the bit that needs to be modified is modified, and the other bits are not modified. The value of the open bit cannot be changed at will. The default value of the register is subject to the value read. The default value of different batches of ICs may be different.

5) MCU operation process: When INT remains high for 100ms, you can read and write the I2C register. You can initialize the register first (modify the register only when special functions need to be modified. If you do not need to modify the register, you do not need to write the register) and then read the internal information of the IC (electricity, power, Charge and discharge state, button state) to perform operations with characteristic requirements (such as special indicator lights, charge and discharge management, fast charge request management); access to I2C needs to be stopped within 16ms after INT is low.

Initialization register configuration example:

A. Charging constant voltage setting, default 4.2V 0x0D=00111100; B.

Maximum power setting, default VBUS1 100W 0x07 bit5:0=101101;

VBUS2 60W 0x21 bit5:0=100100;

C. Battery capacity setting, default 10000mAH 0x08 bit6:0=0110010.

6) The IP5389 register default value is only for customers to refer to the current function configuration. If you need to operate the register, you need to first

Read it out, perform calculations, and then write it back to the register.

7) When the MCU uses IP5389 VCCIO for power supply, the MCU power consumption needs to be less than 20mA.

8) IP5389_I2C_AACC sets the number of battery cells in series by judging the resistance value of the FCAP (pin 40) pin connected to GND, as shown in Table 2 below:

No.40pins connected toGNDresistance (ohm1%)	Number of battery cells in series
27K	6string
18k	5string
13k	4string
9.1k	3string
6.2k	2string

surface2

Version/revision history

Version	date	modify the content	Corresponding firmware	Drafter/reviser
V1.0	2021.10.27	First edition released		XWH
V1.1	2021.11.25	1, removeVBUS1/VBUS2VoltageADC 2, increase the trickle charging current setting		XWH
V1.11	2021.12.06	1, modify the trickle charging current threshold		XWH
V1.2	2022.01.17	1, increase the trickle current value and capacity increase enable	IP5389_I2C_AACC_VAMNK_m.bin IP5389_I2C_AACC_VBUSC_m.bin IP5389_I2C_AACC_VDFPB_m.bin	XWH

3Read/write operation register

3.1 SYS_CTL0(Output and charge enable register)

I2Caddress0XEARegister address =0x00

Bit(s)	Name	Description	R/W	RESET
7	En_load_reg	Wake up after power on and reset register value enable 0:Do not reset register values 1:Reset register value ShouldbitIt is not recommended to change it to0, if it needs to be modified, the software needs to periodically reset the register default value (0X00 bit6Write1),like VINOK VBUOKAfter the signal is triggered	R/W	1
6	En_reset_reg	MCUReset register Write1: Reset the register to the default value. After reset, thebit automatically restore to0	R/W	0
5:4	En_c2b	Whether to enable discharge after charging removal 11: No matter whether the output is loaded or not, it will be turned on by default after charging is removed. start discharge 10: It is detected that there is a load on the output, and the discharge is started after the charge is removed. 01: Directly enter standby state after charging is removed	R/W	11
3	En_ppath	5VEnable charging and discharging at the same time 1: Enable charging and discharging at the same time 0: Turn off charging and discharging at the same time	R/W	1
2	En_ppath_vinloop	Simultaneous charging and discharging automatically increases input undervoltage and enables 1: The input undervoltage loop is4.9V 0: The input undervoltage loop is4.5V	R/W	1
1	En_dc_dc_output	Discharge output enable (cannot output after shutdown) 1:enable 0:disable	R/W	1
0	En_dc_dc_input	Charging input enable (cannot be charged when turned off) 1:enable 0:disable	R/W	1

3.2 DCP_DIG_CTL1_VBUS1(VBUS1port input and output fast charging protocol enable)

I2Caddress0XEARegister address =0x01

Bit(s)	Name	Description	R/W	RESET
7	En_vbus1_sink_afc/fcp	VBUS1mouth inputAFC/FCPFast charging enabled 1:enable 0:disable	R/W	1
6	En_vbus1_src_afc/fcp	VBUS1port outputAFC/FCPFast charging enabled 1:enable 0:disable	R/W	1
5	En_vbus1_sink_pd	VBUS1mouth inputPDFast charging enabled 1:enable 0:disable	R/W	1
4	En_vbus1_ src_pd	VBUS1port outputPDFast charging enabled 1:enable	R/W	1

		0:disable		
3:2		Reserved		XX
1	En_vbus1_sink_qc	VBUS1mouth inputDPDMFast charging enabled 1:enable 0:disable	R/W	0
0	En_vbus1_src_scp	VBUS1mouthSCPOutput enable 1:enable 0:disable	R/W	1

3.3 DCP_DIG_CTL2_VBUS(VBUSport input and outputMOSEnable)

I2Caddress0XEARegister address =0x02

Bit(s)	Name	Description	R/W	RESET
7	En_vbus1_sink_mos	VBUS1mouthMOSInput enable 1:enable 0:disable	R/W	1
6	En_vbus1_src_mos	VBUS1mouthMOSOutput enable 1:enable 0:disable	R/W	1
5	En_vbus2_sink_mos	VBUS2mouthMOSInput enable 1:enable 0:disable	R/W	1
4	En_vbus2_src_mos	VBUS2mouthMOSOutput enable 1:enable 0:disable	R/W	1
3:0		Reserved		XX

3.4 DCP_DIG_CTL3_VBUS2(VBUS2port input and output fast charging protocol enable)

I2Caddress0XEARegister address =0x03

Bit(s)	Name	Description	R/W	RESET
7	En_vbus2_sink_afc/fcp	VBUS2mouth inputAFC/FCPFast charging enabled 1:enable 0:disable	R/W	1
6	En_vbus2_src_afc/fcp	VBUS2port outputAFC/FCPFast charging enabled 1:enable 0:disable	R/W	1
5	En_vbus2_sink_pd	VBUS2mouth inputPDFast charging enabled 1:enable 0:disable	R/W	1
4	En_vbus2_src_pd	VBUS2port outputPDFast charging enabled 1:enable 0:disable	R/W	1
3:2		Reserved		XX
1	En_vbus2_sink_qc	VBUS2mouth inputDP DMFast charging enabled 1:enable 0:disable	R/W	0
0	En_vbus2_src_scp	VBUS2mouthSCPOutput enable 1:enable 0:disable	R/W	1

3.5 DCP_DIG_CTL4_VOUT1(VOUT1port output fast charging protocol enabled)

I2Caddress0XEARegister address =0x04

Bit(s)	Name	Description	R/W	RESET
7	En_vout1_src_scp	VOUT1mouthSCPLow voltage output enable 1:enable 0:disable	R/W	1
6		Reserved		XX
5	En_vout1_src_vooc	VOUT1mouthVOOCEnable 1:enable 0:disable	R/W	1
4:2		Reserved		XX
1	En_vout1_det	VOUT1Load detection enabled 1:enable 0:disable	R/W	1
0	En_vout1_src_mos	VOUT1 MOSOutput enable 1:enable 0:disable	R/W	1

3.6 DCP_DIG_CTL5_VOUT2(VOUT2port output fast charging protocol enabled)

I2Caddress0XEARegister address =0x05

Bit(s)	Name	Description	R/W	RESET
7	En_vout2_src_scp	VOUT2mouthSCPLow voltage output enable 1:enable 0:disable	R/W	1
6		Reserved		XX
5	En_vout2_src_vooc	VOUT2mouthVOOCEnable 1:enable 0:disable	R/W	1
4:2		Reserved		XX
1	En_vout2_det	VOUT2Load detection enabled 1:enable 0:disable	R/W	1
0	En_vout2_src_mos	VOUT2 MOSOutput enable 1:enable 0:disable	R/W	1

3.7 SYS_CTL6(Output port control register)

I2Caddress0XEARegister address =0x06

Bit(s)	Name	Description	R/W	RESET
7	Force_sleep	Write1back100ms IP5389Directly enter the shutdown state,VINOK orVBUSOKtime to write1It won't go to sleep	R/W	0
6	Force_det_src	Write1Exit fast charging and recheck all output ports	R/W	0
5	Force_vbus1_det	Write1,recheckVBUS1port, open if there is loadVBUS1 If there is no load on the port, it will not be opened.VBUS1mouth	R/W	0
4	Force_vbus2_det	Write1,recheckVBUS2port, open if there is loadVBUS2 If there is no load on the port, it will not be opened.VBUS2mouth	R/W	0

3	Force_vout1	Write1,500msrestart afterVOUT1mouth, no need to retest	R/W	0
2	Force_vout1_det	Write1,recheckVOUT1port, open if there is loadVOUT1 If there is no load on the port, it will not be opened.VOUT1mouth	R/W	0
1	Force_vout2	Write1,500msrestart afterVOUT2mouth, no need to retest	R/W	0
0	Force_vout2_det	Write1,recheckVOUT2port, open if there is loadVOUT2 If there is no load on the port, it will not be opened.VOUT2mouth	R/W	0

3.8 SYS_CTL7(VBUS1Maximum power select register)

I2Caddress0XEARegister address =0x07

Bit(s)	Name	Description	R/W	RESET
7:6		Reserved		XX
5:3	Vbus1_sink_power	VBUS1Input power selection: 000:27W 001:30W 010:45W 011:60W 100:65W 101:100W	R/W	101
2:0	Vbus1_src_power	VBUS1Output power selection: 000:27W 001:30W 010:45W 011:60W 100:65W 101:100W	R/W	101

65Wand100WNeed to addMarkIdentify the circuit.

3.9 SYS_CTL8(Battery capacity register)

I2Caddress0XEARegister address =0x08

Bit(s)	Name	Description	R/W	RESET
7		Reserved		XX
6:0	En_fcap	Cell capacityFCAP FACP=N*200mah *Battery capacity of a single cell, default10000mAH	R/W	0110010

3.10 SYS_CTL9(Light load shutdown time setting)

I2Caddress0XEA Register address =0x09

Bit(s)	Name	Description	R/W	RESET
7	En_ilow	Light load shutdown enable 1:enable 0:disable	R/W	1
6:0	Set_ilow_time	Light load shutdown time setting (default32s) N*8S	R/W	0000100

3.11 SYS_CTL10(Light load shutdown power setting)

I2Caddress0XEA Register address =0x0A

Bit(s)	Name	Description	R/W	RESET

7	En_power_ilow	Light load shutdown optionVSYSPower enable 1:enable(At loads less than0.3Wlight load shutdown) 0: disable	R/W	1
6:0	Set_power_ilow	IsysLight load shutdown output power threshold setting (default 300mW) POW_LOW=N *5mW	R/W	0111100

3.12 SYS_CTL11(Light load shutdown current setting)

I2Caddress0XEA Register address =0x0B

Bit(s)	Name	Description	R/W	RESET
7	En_isys_ilow	Light load shutdown optionVSYSCurrent enable 1:enable(less than85mAJust light load shutdown) 0:disable	R/W	0
6:0	Set_isys_ilow	IsysLight load shutdownADCOutput current threshold setting ISYS_LOW=N*2 mA	R/W	0101000

3.13 SYS_CTL12(Charging stop setting)

I2Caddress0XEA Register address =0x0C

Bit(s)	Name	Description	R/W	RESET
7	En_batlowhold	Charging activation enable 1:enable 0:disable	R/W	0
6	En_int_low	IP5389When there is something unusualINTpull down2MShintMCUAn abnormality occurs 1:enable 0:disable	R/W	0
5	En_stop_chg	Charging stop and charging enable 1:Normal charging stop 0: Keep charging	R/W	1
4	En_batlow	Low battery voltage selection setting 0: Single battery low voltage (determined by0x0E bit5:3set up) 1: total battery low voltage (determined by0x2C bit7:0set up)	R/W	0
3:0		Reserved		XX

3.14 SYS_CTL13(Charging constant voltage setting)

I2Caddress0XEA Register address =0x0D

Bit(s)	Name	Description	R/W	RESET
7:0	En_vset_chg	Charging constant voltage setting (3600mV-4400mV,default4200mV) VSET=N*10+3600mV		0X3C

3.15 SYS_CTL14(Key switch mode setting)

I2Caddress0XEA Register address =0x0E

Bit(s)	Name	Description	R/W	RESET
7:6		Reserved		XX
5:3	Set_batlow	Battery low voltage setting 000:2.75V*N 001:2.85V*N 010:2.95V*N		011

		011:3.05V*N 100:3.15V*N N:Number of battery cells in series		
2:0	Key_mode	Key switch mode setting 000:disable 001:Vibration switch 010:Short press to turn on, long press2sShut down, double-click to turn on the flashlight 011: Short press to turn on, double press to turn on and off the flashlight, no button to turn off 100: Short press to turn on, long press2sTurn the flashlight on and off without pressing a button 101: Short press to turn on, double click to turn off, long press2sSwitch flashlight	R/W	101

3.16 SYS_CTL15(VBUS2Maximum power select register)

I2Caddress0XEARegister address =0x21

Bit(s)	Name	Description	R/W	RESET
7:6		Reserved		XX
5:3	Vbus2_sink_power	VBUS2Input power selection: 000:18W 001:27W 010:30W 011:45W 100:60W	R/W	100
2:0	Vbus2_src_power	VBUS2Output power selection: 000:18W 001:27W 010:30W 011:45W 100:60W	R/W	100

3.17 TYPEC_CTL16(PDcontrol register)

I2Caddress0XEARegister address =0X22

Bit(s)	Name	Description	R/W	RESET
7:6	Vbus1_mode_selL	VBUS1 CCMode selection 00:UFP 01:DFP 11:DRP	R/W	11
5:4	Vbus2_mode_selL	VBUS2CCMode selection 00:UFP 01:DFP 11:DRP	R/W	11
3	En_vbus_ck	Type-C SRCAfter the output connection is successfulCThe port is always open and enabled 1:enable 0:disable	R/W	0
2:0		Reserved	R/W	XX

3.18 TYPEC_CTL17(outputPDOcurrent setting register)

I2Caddress0XEA Register address =0x23

Bit(s)	Name	Description	R/W	RESET

7	En_5vpdo_3A/2.4A	5VPDOCurrent setting 1:3A 0:2.4A	R/W	1
6	En_pps2pdo_iset	PPS2 PDOCurrent setting enable 1:enable 0:disable * After enabling, the output power and overcurrent are set byPDOThe current is based on the setting, and the overcurrent is based on the settingPDOcurrent1.1times	R/W	0
5	En_pps1pdo_iset	PPS1 PDOCurrent setting enable 1:enable 0:disable * After enabling, the output power and overcurrent are set byPDOThe current is based on the setting, and the overcurrent is based on the settingPDOcurrent1.1times	R/W	0
4	En_20vpdo_iset	20VPDOCurrent setting enable 1:enable 0:disable * After enabling, the output power and overcurrent are set byPDOThe current is based on the setting, and the overcurrent is based on the settingPDOcurrent1.1times	R/W	0
3	En_15vpdo_iset	15VPDOCurrent setting enable 1:enable 0:disable * After enabling, the output power and overcurrent are set byPDOThe current is based on the setting, and the overcurrent is based on the settingPDOcurrent1.1times	R/W	0
2	En_12vpdo_iset	12VPDOCurrent setting enable 1:enable 0:disable * After enabling, the output power and overcurrent are set byPDOThe current is based on the setting, and the overcurrent is based on the settingPDOcurrent1.1times	R/W	0
1	En_9vpdo_iset	9VPDOCurrent setting enable 1:enable 0:disable * After enabling, the output power and overcurrent are set byPDOThe current is based on the setting, and the overcurrent is based on the settingPDOcurrent1.1times	R/W	0
0	En_5vpdo_iset	5VPDOCurrent setting enable 1:enable 0:disable	R/W	0

3.19 TYPEC_CTL18(5VPDOcurrent setting register)

I2Caddress0XEA Register address =0x24

Bit(s)	Name	Description	R/W	RESET
7:0	5vpdo_iset	5VPDOCurrent setting 5VPDO=20mA*N (default3A,Max=3A)	R/W	0x96

3.20 TYPEC_CTL19(9VPDOcurrent setting register)

I2Caddress0XEA Register address =0x25

Bit(s)	Name	Description	R/W	RESET
7:0	9vpdo_iset	9VPDOCurrent setting 9VPDO=20mA*N (default3A,Max=3A)	R/W	0x96

3.21 TYPEC_CTL20(12VPDOcurrent setting register)

I2Caddress0XEA Register address =0x26

Bit(s)	Name	Description	R/W	RESET
7:0	12vpdo_iset	12VPDOCurrent setting 12VPDO=20mA*N(default3A,Max=3A)	R/W	0x96

3.22 TYPEC_CTL21(15VPDOcurrent setting register)

I2Caddress0XEA Register address =0x27

Bit(s)	Name	Description	R/W	RESET
7:0	15vpdo_iset	15VPDOCurrent setting 15VPDO=20mA*N(default3A,Max=3A)	R/W	0x96

3.23 TYPEC_CTL22(20VPDOcurrent setting register)

I2Caddress0XEA Register address =0x28

Bit(s)	Name	Description	R/W	RESET
7:0	20vpdo_iset	20VPDOCurrent setting 20VPDO=20mA*N(default5A, need to identify emark,Max=5A)not recognizedmarkfor3A	R/W	0xFA

3.24 TYPEC_CTL23(PPS1 PDOcurrent setting register)

I2Caddress0XEA Register address =0x29

Bit(s)	Name	Description	R/W	RESET
7:0	Pps1pdo_iset	PPS1 PDOCurrent setting PPS1 PDO=50mA*N(default5A, need to identify emark,Max=5A)not recognizedmarkfor3A	R/W	0x64

3.25 TYPEC_CTL24(PPS2 PDOcurrent setting register)

I2Caddress0XEA Register address =0x2A

Bit(s)	Name	Description	R/W	RESET
7:0	Pps2pdo_iset	PPS2 PDOCurrent setting PPS2 PDO=50mA*N(default5A, need to identify emark,Max=5A)not recognizedmarkfor3A	R/W	0x64

3.26 TYPEC_CTL25(outputPDOsetting register)

I2Caddress0XEA Register address =0x2B

Bit(s)	Name	Description	R/W	RESET
7		Reserved	R/W	R
6	En_src_pps2pdo	PPS2 PDOEnable 1:enable 0:disable *disableno afterPPS2 PDO	R/W	1
5	En_src_pps1pdo	PPS1 PDOEnable 1:enable 0:disable	R/W	1

		*disableno afterPPS1 PDO		
4	En_src_20vpdo	20VPDOEnable 1:enable 0:disable *disableno after20V PDO	R/W	1
3	En_src_15vpdo	15VPDOEnable 1:enable 0:disable *disableno after15V PDO	R/W	1
2	En_src_12vpdo	12VPDOEnable 1:enable 0:disable *disableno after12V PDO	R/W	1
1	En_src_9vpdo	9VPDOEnable 1:enable 0:disable *disableno after9V PDO	R/W	1
0		Reserved	R/W	R

3.27 SYS_CTL18(Battery low voltage setting)

I2Caddress0XEA Register address =0x2C

Bit(s)	Name	Description	R/W	RESET
7:0	Set_batlow	Battery low voltage setting (3300-25600mV) batlow =N*100mV	R/W	0X9C

3.28 SYS_CTL19(Trickle charging current setting)

I2Caddress0XEA Register address =0x2D

Bit(s)	Name	Description	R/W	RESET
7:4	Set_iset_tk	Charging current at battery terminal during trickle flowiset(default0.2A) Battery terminal trickle charging current =iset*0.1A+0.1A	R/W	0001
3	En_fcap	Capacity increase multiple enable 1:enable 0:disable * After enabling, the capacity is0x08 bit6:0Let the value be multiplied by0x2D bit2value, maximum65000mAH.	R/W	0
2	Set_fcap	Capacity increase multiple 1:3times 0:2times	R/W	0
1	En_iset_tk	Trickle charging current increase multiple enable 1:enable 0:disable * After enabling, the trickle charging current is0x2D bit7:4Let the value be multiplied by 0x2D bit0value.	R/W	0
0	Set_iset_tk	Trickle charge current increase multiple 1:3times 0:2times	R/W	0

4read-only status indication register

4.1 SOC_CAP_DATA(Cell power data register)

I2Caddress0XEARegister address =0X30

Bit(s)	Name	Description	R/W
7:0	Soc_cap	Cell percentage power data (%) SOC_CAP=N	R

4.2 STATE_CTL0(Charge status control register)

I2Caddress0XEARegister address =0X31

Bit(s)	Name	Description	R/W
7	Output_mos_state	outputMOSstate 1: Has any output portMOSOn state 0: No output portMOSOn state	R
6	Chg_en	Charging status flag 1: Charging enable has been turned on and charging is normal. 0: There is currently input voltage and charging is not enabled.	R
5	Chg_en	Charging flag 1:charging(VBUSOKEven in charging state) 0: Discharge state	R
4	Chg_end	full status flag 1: Charging is fully charged 0: Charging is not fully charged	R
3	Output_en	Discharge status flag 1: Discharge state and the output port is open, without any abnormality 0: The discharge status output is not turned on or there is a discharge abnormality.	R
2:0	Chg_state	Chg_state 000: Standby 001: Trickle 010: Constant current charging 011: Constant voltage charging 100: Waiting for charging (including charging not turned on, etc.) 101: full status 110: Charging timeout	R

4.3 STATE_CTL1(Charge status control register)

I2Caddress0XEARegister address =0X32

Bit(s)	Name	Description	R/W
7:6	Chg_state	Chg_state 00:Single port input5VCharge 01:Single port input high voltage fast charging 10: Charge and release simultaneously5VCharge	R
0		Reserved	R

4.4 STATE_CTL2(input status control register)

I2Caddress0XEARegister address =0X33

Bit(s)	Name	Description	R/W
7	Vbus1_ok	VBUS1OK 1:VBUS1There is electricity 0:VBUS1no power	R
6	Vbus1_ov	VBUS1OV 1:VBUS1Input overvoltage 0:VBUS1There is no overvoltage on the input	R
5	Vbus2_ok	VBUS2OK 1:VBUS2There is electricity 0:VBUS2no power	R
4	Vbus2_ov	VBUS2OV 1:VBUS2Input overvoltage 0:VBUS2There is no overvoltage on the input	R
3		Reserved	
2:0	Vchg_state	Charging voltage 111:20VCharge 110:15VCharge 101:12VCharge 100:9VCharge 011:7VCharge 010:5VCharge	R

4.5 VBUS1_STATE0(VBUS1status indication register)

I2Caddress0XEARegister address =0X34

Bit(s)	Name	Description	R/W
7	Vbus1_sink_ok	VBUS1 SINKInput connection flag 1:efficient 0:invalid	R
6	Vbus1_src_ok	VBUS1 SRCOutput connection flag 1:efficient 0:invalid	R
5	Vbus1_src_pd_ok	VBUS1 Src_Pd_OkOutput connection flag 1 :efficient 0:invalid	R
4	Vbus1_sink_pd_ok	VBUS1 Sink_Pd_OkInput connection flag 1 :efficient 0:invalid	R
3	Vbus1_sink_qc_ok	VBUS1Enter the fast charging valid flag bit(QC5VandPD5VNot counting fast chargingOK) 1:efficient 0:invalid	R
2	Vbus1_src_qc_ok	VBUS1Output fast charge valid flag bit(QC5VandPD5VNot counting fast chargingOK) 1:efficient 0:invalid	R
1:0		Reserved	R

4.6 MOS_STATE(output inputMOSstatus indication register)

I2Caddress0XEARegister address =0X35

Bit(s)	Name	Description	R/W
7	At_same	Simultaneous charging and simultaneous release flag 0: Not charging and depositing at the same time 1: Charge and release at the same time	R
6	Mos_vbus1_sink	VBUS1mouth inputMOS state 0:Disabled 1: On state	R
5	Mos_vbus2_sink	VBUS2mouth inputMOS state 0:Disabled 1: On state	R
4	Mos_vbus1_src	VBUS1port outputMOS state 0:Disabled 1: On state	R
3	Mos_vout2	Vout2port outputMOS state 0:Disabled 1: On state	R
2	Mos_vout1	Vout1port outputMOS state 0:Disabled 1: On state	R
1	Isys_low	IsysOutput current light load flag 1:efficient 0:invalid	R
0	Psys_low	psysOutput power light load flag 1:efficient 0:invalid	R

4.7 KEYIN_STATE(Key status indication register)

I2Caddress0XEARegister address =0X36

Bit(s)	Name	Description	R/W
7	On_off_long	long press button2SThe flag needs to be written1clear0 1:efficient 0:invalid	R
6	On_off_2short	The flag needs to be written when the button is pressed twice consecutively.1 clear0 1:efficient 0:invalid	R
5	On_off_short	The button short press flag needs to be written1 clear0 1:efficient 0:invalid	R
4:0		Reserved	R

4.8 VBUS2_STATE0(VBUS2status indication register)

I2Caddress0XEARegister address =0X37

Bit(s)	Name	Description	R/W
7	Vbus2_Sink_ok	VBUS2 SINKInput connection flag	R

		1:efficient 0:invalid	
6	Vbus2_Src_ok	VBUS2 SRCOutput connection flag 1:efficient 0:invalid	R
5	Vbus2_Src_pd_ok	VBUS2 Src_Pd_OkOutput connection flag 1 :efficient 0:invalid	R
4	Vbus2_Sink_pd_ok	VBUS2 Sink_Pd_OkInput connection flag 1 :efficient 0:invalid	R
3	Vbus2_Sink_qc_ok	VBUS2Enter the fast charging valid flag bit(QC5VandPD5VNot counting fast chargingOK) 1:efficient 0:invalid	R
2	Vbus2_Src_qc_ok	VBUS2Output fast charge valid flag bit(QC5VandPD5VNot counting fast chargingOK) 1:efficient 0:invalid	R
1	Mos_vbus2_src	VBUS2port outputMOSstate 0:Disabled 1: On state	R
0		Reserved	R

4.9 STATE_CTL3(System overcurrent indication register)

I2Caddress0XEARegister address =0X38

Bit(s)	Name	Description	R/W
7:6		Reserved	R
5	Vsys_oc	VSYSOutput overcurrent flag bit, needs to be written1clear0 1:VSYSThe output has a trigger overcurrent signal 0:VSYSThe output does not trigger an overcurrent signal When the first short circuit signal is detected, first write1clear0, and then read again, if600msIf the overcurrent signal is detected twice or more continuously within a period, the overcurrent signal is considered valid.	R
4	Vsys_scdt	VSYSOutput short circuit flag, need to write1clear0 1:VSYSThe output has a trigger short circuit signal 0:VSYSThe output does not trigger a short circuit signal When the first short circuit signal is detected, first write1clear0, and then read again, if600msIf the short-circuit signal is detected twice or more continuously within a period, the short-circuit signal is considered valid.	R
3:0		Reserved	R

4.10 IVBUS2_IADC_DAT0(IVBUS2output current register)

I2Caddress0XEARegister address =0X4E

Bit(s)	Name	Description	R/W
7:0	IVBU2SADC[7:0]	IVBUS2Output current data for the low8bit IVBUS2ADCOutput current	R

4.11 IVBUS2_IADC_DAT1(IVBUS2output current register)

sendI2Caddress0XEARegister address =0X4F

Bit(s)	Name	Description	R/W
7:0	IVBU2SADC [15:8]	IVBUS2Output current data of high8bit IVBUS2ADCOutput current IVBUS2= IVBUS2ADC*0.548mA	R

4.12 BATVADC_DAT0(VBATvoltage register)

I2Caddress0XEARegister address =0X50

Bit(s)	Name	Description	R/W
7:0	BATVADC[7:0]	BATVADCdata low8bit VBATPINvoltage	R

4.13 BATVADC_DAT1(VBATvoltage register)

I2Caddress0XEARegister address =0X51

Bit(s)	Name	Description	R/W
7:0	BATVADC[15:8]	BATVADChigh data8bit VBATPINvoltage VBAT=BATVADC*2.6855mV	R

4.14 VSYSVADC_DAT0(VSYSvoltage register)

I2Caddress0XEARegister address =0X52

Bit(s)	Name	Description	R/W
7:0	VSYSVADC[7:0]	VSYSVoltage data of low8bit VSYSPINvoltage	R

4.15 VSYSVADC_DAT1(VSYSvoltage register)

sendI2Caddress0XEARegister address =0X53

Bit(s)	Name	Description	R/W
7:0	VSYSVADC[15:8]	VSYSHigh voltage data8bit VSYSPINvoltage VSYS= VSYSVADC*2.1484375mV	R

4.16 IVBUS_IADC_DAT0(input current register)

I2Caddress0XEARegister address =0X54

Bit(s)	Name	Description	R/W
7:0	IVBUSADC[7:0]	The charging input current data is low8bit VBUSinput current	R

4.17 IVBUS_IADC_DAT0(input current register)

sendI2Caddress0XEARegister address =0X55

Bit(s)	Name	Description	R/W
7:0	IVBUSADC [15:8]	The charging input current data is high8bit VBUSinput current Iin= IVBUSADC*0.548 mA	R

4.18 IVOUT1_IADC_DAT0(VOUT1output current register)

I2Caddress0XEARegister address =0X56

Bit(s)	Name	Description	R/W
7:0	IVOUT1ADC[7:0]	VOUT1Output current data for the low8bit VOUT1Output current	R

4.19 IVOUT1_IADC_DAT1(VOUT1output current register)

sendI2Caddress0XEARegister address =0X57

Bit(s)	Name	Description	R/W
7:0	IVOUT1ADC [15:8]	VOUT1Output current data of high8bit VOUT1Output current IOUT1= IVOUT1ADC*0. 548mA	R

4.20 IVOUT2_IADC_DAT0(VOUT2output current register)

I2Caddress0XEARegister address =0X58

Bit(s)	Name	Description	R/W
7:0	IVOUT2ADC[7:0]	VOUT2Output current data for the low8bit VOUT2Output current	R

4.21 IVOUT2_IADC_DAT1(VOUT2output current register)

sendI2Caddress0XEARegister address =0X59

Bit(s)	Name	Description	R/W
7:0	IVOUT2ADC [15:8]	VOUT2Output current data is high8bit VOUT2Output current IOUT2= IVOUT2ADC*0.548mA	R

4.22 IVBUS1_IADC_DAT0(IVBUS1output current register)

I2Caddress0XEARegister address =0X5A

Bit(s)	Name	Description	R/W
7:0	IVBU1SADC [7:0]	IVBUS1Output current data for the low8bit IVBUS1ADCOutput current	R

4.23 IVBUS1_IADC_DAT1(IVBUS1output current register)

sendI2Caddress0XEARegister address =0X5B

Bit(s)	Name	Description	R/W
7:0	IVBU1SADC [15:8]	IVBUS1Output current data of high8bit IVBUS1ADCOutput current IVBUS1= IVBUS1ADC*0.548mA	R

4.24IBATIADC_DAT0(BATterminal current register)

I2Caddress0XEARegister address =0x6E

Bit(s)	Name	Description	R/W
7:0	IBATIADC[7:0]	Cell terminal currentIBATIADCdata low8bit	R

4.25IBATIADC_DAT1(BATterminal current register)

I2Caddress0XEARegister address =0x6F

Bit(s)	Name	Description	R/W
7:0	IBATIADC[15:8]	Cell terminal currentBATIADChigh data 8bit IBAT= IBATIADC*1.096mA	R

4.26 IVSYS_IADC_DAT0(VSYSterminal current register)

I2Caddress0XEARegister address =0x70

Bit(s)	Name	Description	R/W
7:0	IVSYSADC[7:0]	IVSYSterminal currentIVSYSADCdata low8bit	R

4.27 IVSYS_IADC_DAT1(VSYSterminal current register)

I2Caddress0XEARegister address =0x71

Bit(s)	Name	Description	R/W
7:0	IVSYSADC[15:8]	IVSYSterminal currentIVSYSADChigh data 8bit IVSYS = IVSYSADC*1.096mA	R

4.28 VSYS_POW_DAT0(VSYSterminal power register)

I2Caddress0XEARegister address =0X74

Bit(s)	Name	Description	R/W
7:0	VSYS_POW_ADC [7:0]	VSYSTerminal powerADCdata low8bit	R

4.29 VSYS_POW_DAT1(VSYSterminal power register)

I2Caddress0XEARegister address =0X75

Bit(s)	Name	Description	R/W
7:0	VSYS_POW_ADC[15:8]	VSYSTerminal powerADChigh data8bit VSYS_POW= VSYS_POW_ADC*19.292mW	R

4.30 FCAP_DAT0(FCAPcapacity register)

I2Caddress0XEARegister address =0X76

Bit(s)	Name	Description	R/W
7:0	FCAP_ADC[7:0]	current capacityADCdata low8bit FCAP=N	R

4.31 FCAP_DAT1(FCAPcapacity register)

I2Caddress0XEARegister address =0X77

Bit(s)	Name	Description	R/W
7:0	FCAP_ADC[15:8]	current capacityADChigh data8bit FCAP=N	R

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